Subsystems for Data Acquisition
Analog-to-Digital Converter
IEEE-488 Function Card

Project 39 Team: Dana Baumann
Daniel Bruhn

Spring 2005
TABLE OF CONTENTS

I.  Executive Summary ........................................................................................................... 3
II.  Newsletter ......................................................................................................................... 5

III.  Project Report ................................................................................................................. 6
     A.  Introduction .................................................................................................................. 6
     B.  Background .................................................................................................................. 7
     C.  Product Requirements ............................................................................................... 8
     D.  Design Alternatives .................................................................................................... 10
     E.  Design Specifications .................................................................................................. 12
     F.  Design Description ...................................................................................................... 15
     G.  Construction Details ................................................................................................... 22
     H.  Costs ............................................................................................................................. 24
     I.  Conclusions .................................................................................................................. 25

IV.  User Instructions ............................................................................................................. 26

Appendices ............................................................................................................................ 27

Project Notebook
I. Executive Summary

This project involved the design and construction of a high-speed analog-to-digital converter (ADC) card for an IEEE-488 interface box. The IEEE-488 interface box was built by Dr. Kolbas, an Electrical and Computer Engineering professor at North Carolina State University, and was provided for this project. This ADC Function Card was used to implement a computer-based spectrum analyzer written in HP-Basic. It accepts analog input signals to sample in the range from 10 Hz to 25 kHz with a voltage range from +10V to –10V, samples the input signal with 16 bits of precision at a user-selected rate of 10 kHz or 100 kHz, and outputs the sampled data in byte-wise big-endian format over the IEEE-488 bus to the computer. The HP-Basic program then computes the Discrete Fourier Transform on the sampled data.

The ADC Function Card was designed with Orcad Capture and Microsoft Visio 2003, prototyped on a breadboard, and implemented on a through-hole circuit board with the wire-wrap technique. Its primary components are two Butterworth Low-Pass filters to anti-alias the user-supplied input signal, one double-pole-double-throw (DPDT) relay to select the appropriate filtered signal based on the sampling rate, one ADC chip to perform the sampling via successive-approximation, one PIC microcontroller to control the whole card, one 32K x 8 SRAM chip to store the sampled data until the computer is ready, one 74LS373 octal transparent latch to drive the bus data lines, and a Talk/Listen Circuit of several components (IC’s: three 74LS85 comparators, one DIP switch, one 74LS74 latch) to detect Talk and Listen assignments from the computer over the IEEE-488 bus. The following figure shows the basic block diagram of the ADC Card:

![Figure 1: Block Diagram](image-url)
The ADC Function Card was produced at a very low cost ($102) and successfully constructed. Dr. Kolbas will use it to isolate various frequencies of signals from the instruments in his lab and view them on the HP computer.
II. Newsletter

Are you a dog owner who can’t get your pet to stop howling? Do you suspect a dog whistle operated by the bratty kid next door? Then have we got a product for you! What you need is our handy-dandy Analog-to-Digital IEEE-488 Function Card!

It couldn’t be easier: Just insert the conveniently-labeled A/D Converter Card into your custom IEEE-488 (HP GPIB) interface box, attach a microphone and amplifier circuit to the card input, fire up your trusty HP 9000/300 series PC, load the provided HP-Basic Fourier Analysis software, and away you go! With our spiffy application, you can detect frequencies we humans can’t hear but your dog can! If you see a frequency spike above 15 kHz, then you know you’ve caught that neighborhood brat.

Our ADC card is hand-crafted with the finest wire-wrap technique since 1975. We use only the highest-quality free sample components, pilfered from leading manufacturers in the electronics industry: Texas Instruments, Microchip, and Rudy’s Electronics Shop. A convenient bi-color status light, adjustable gain & offset potentiometers, and two selectable sampling rates add to the already-jam-packed functionality of this device! With such careful craftsmanship, you might expect to pay $1000 for such a wonder of the electronics world.

Well, we’d love to sell it to you for $1000, but this card was custom-built for Dr. Robert Kolbas, a professor in the Electrical and Computer Engineering Department at North Carolina State University. Dr. Kolbas is on the cutting edge of signals research, and was in need of a simple spectrum analyzer for his instruments. With our sharp minds and adept fingers, we designed and constructed this analog-to-digital function card for his use. Now all is well at Kolbas Labs, where the future is being made today.
III. Project Report

A. Introduction

The purpose of this project was to design and build a function card for a custom IEEE-488 interface box constructed by our sponsor, Dr. Robert Kolbas. The card we chose would add extra capability to the box and assist Dr. Kolbas in his research. From the list of possible cards we selected the Analog-to-Digital Converter and inserted some of the specifications from the Spectrum Analyzer Card to augment its functionality. We designed the card to sample with 16-bit resolution, offer selectable sampling rates of 10 and 100 kHz, support input signals from 10 Hz to 25 kHz and +10 V to –10 V (for more details see the Product Requirements). With this function card and an HP-Basic Discrete Fourier Transform program, Dr. Kolbas will be able to distinguish signals of varying frequencies emitted from his instruments.

The NCSU Electrical and Computer Engineering Department, in which Dr. Kolbas is a professor, was our project sponsor. Our team members were Dana Baumann and Daniel Bruhn. Due to the small size of our team, complete division of roles was not possible. However, in general Dana Baumann handled component acquisition, prototype assembly, wire-wrap construction, and documentation, while Daniel Bruhn dealt with technical design, prototype assembly, layout, soldering, testing, and documentation.
B. Background

Dr. Kolbas and his graduate students operate interface boxes that contain slots for expansion via multiple function cards. These boxes utilize the IEEE-488 (formerly Hewlett-Packard GPIB) protocol to communicate with an external computer, and a customized IEEE-488 protocol to communicate internally among the inserted cards:

![Figure 2: IEEE-488 box](image)

Dr. Kolbas was in need of a spectrum analyzer to distinguish his instrument output signals from 60 Hz noise and other such interference. With an analog-to-digital converter card inserted into one of the IEEE-488 boxes, an analog input signal could be supplied and the sampled data interpreted on a computer-based spectrum analyzer. As such, our team resolved to design and build such a card to aid Dr. Kolbas with his research.
C. Product Requirements

During the product requirement phase, the team members and the sponsor discussed and agreed upon the technical requirements for product completeness. Below is a list of the requirements for this project:

General Function

(R-1) The ADC card will communicate with the computer via the sponsor's version of the IEEE-488 communication protocol.

(R-2) The ADC card will accept IEEE 488 commands from the computer to:
   a) Set the sampling rate.
   c) Transmit the sampled data.

(R-3) The ADC card will acquire a predefined number of 16-bit samples (8192).

Signal Input Format

(R-4) The ADC card will accept analog input signals to sample in the range from 10Hz to 25kHz.

(R-5) The ADC card will accept analog input signals to sample with a voltage range of +/- 10V.

Output Format

(R-6) The ADC card will sample the input signal with 16 bits of precision (15 bits + sign bit) and output the sampled data over the IEEE 488 interface to the computer, byte-by-byte.

Platform

(R-7) The ADC card circuitry will be implemented using the wire-wrap technique.

(R-8) All integrated circuits on the ADC card will be mounted in sockets.

Packaging

(R-9) The ADC card will be compatible with the sponsor's proprietary cabinet specifications, IEEE 488 interface, and power supply.

(R-10) The ADC card hardware will consist of:
   a) A front panel with the input signal connector and status lights.
   b) Board on which the circuitry is implemented.
   c) Hardware to mount the board to the front panel.
   d) An edge connector on the back of the board to connect to the cabinet's interface.

Power

(R-11) The ADC card will operate on the +/-15V and +5 V power supplied by the internal cabinet bus.

Cost

(R-12) The ADC card will be reproducible for less than $250.
User-Interface

(R-13) The ADC card front panel will have a connector to which the analog input signal may be supplied

(R-14) The ADC card front panel will have an LED status indicator (ready/currently sampling/data acquired).
D. Design Alternatives

During the design phase and preparation for critical design review, the following design alternatives were taken into consideration and analyzed for best engineering practice and best product requirement compliance:

<table>
<thead>
<tr>
<th>Category</th>
<th>Alternative #1</th>
<th>#2</th>
<th>#3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Method for accommodating multiple sampling rates</td>
<td>Multiple Low-pass Time-Continuous Filters</td>
<td>Adjustable Switched-Capacitor Low-pass Filter</td>
<td></td>
</tr>
<tr>
<td>Type of Filter</td>
<td>Butterworth</td>
<td>Bessel</td>
<td>Chebyshev</td>
</tr>
<tr>
<td>ADC Implementation</td>
<td>ADC Chip</td>
<td>Custom Circuitry</td>
<td></td>
</tr>
<tr>
<td>Memory size</td>
<td>x16 bit RAM</td>
<td>x8 bit RAM</td>
<td></td>
</tr>
<tr>
<td>Controller</td>
<td>Pure Hardware</td>
<td>Microcontroller</td>
<td></td>
</tr>
<tr>
<td>Type of Microcontroller</td>
<td>PIC</td>
<td>M16C</td>
<td>AVR</td>
</tr>
<tr>
<td>Programming Language</td>
<td>Assembly</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>Construction Technology</td>
<td>PCB</td>
<td>Wire-Wrap</td>
<td></td>
</tr>
<tr>
<td>IC Attachment</td>
<td>Sockets</td>
<td>Soldering</td>
<td></td>
</tr>
<tr>
<td>IEEE-488 Implementation</td>
<td>IEEE488 w/ software</td>
<td>IEEE488 Circuitry</td>
<td></td>
</tr>
</tbody>
</table>

Below are short rationales for each option chosen (designated by **bold** text):

**Low-pass Filter (s): **Multiple Time-Continuous vs. Adjustable Switched-Capacitor

- The switched-capacitor filter can produce an artificial signal
- “Multiple” in our case is only 2

**Butterworth vs. Bessel vs. Chebyshev**

- Butterworth gives best performance for simplest circuit
- Chebyshev has too much ripple in passband
- Bessel stopband attenuation is too low
- Sponsor does not expect much high-frequency noise (which would be a problem for Butterworth)

**ADC Chip vs. Custom Circuitry**

- Wide variety of ADC chips from which to choose
- Why reinvent the wheel?
- Reliability
- Easier to debug

**RAM width: x16 bits vs. x8 bits**

- x16 chips aren’t free
- IEEE488 bus only supports byte-at-a-time
- ADC chip can output each byte separately

**Hardware vs. Microcontroller**

- Easier to debug
- Familiarity with microcontrollers
- Facilitates timing implementation

**PIC vs. M16C vs. AVR**

- M16C is 16 bit architecture – too much power
- Already have PIC development environment
- Sponsor has experience with PICs
Assembly vs. C
- PIC Assembly is not difficult
- Microchip C compiler only optimizes for 60 days
- Sensitive timing is easier to implement at low level

PCB vs. Wire-Wrap
- PCB is difficult to rework
- Research (not commercial) product
- Easier for sponsor to modify

Sockets vs. Soldering
- May need to replace chips
- Microcontroller will be replaced often (for reprogramming)

IEEE488: Software vs. Circuitry
- Handshaking = tedium
- Consistency (sponsor utilizes circuitry on other cards)
- Circuitry already designed and implemented

Sampling Rate Alternatives
- Fixed sampling rate (100 kHz) w/ 8K (8192) data points
  - Pros: easy; bus can handle data; good resolution (samples/period)
  - Cons: very few periods obtained at low-frequency input signals
- Fixed sampling rate (100 kHz) w/ 32K (32768) data points
  - Pros: good resolution; captures 3 periods of 10 Hz signal; easy
  - Cons: bus can't handle so much data
- Fully-adjustable sampling rate w/ 8K data points
  - Pros: user can adjust sampling rate according to needs
  - Cons: tricky, need switch-capacitor filter (artificial signal)
- Two sampling rates (10 kHz & 100 kHz) w/ 8K data points
  - Pros: easy to implement (need only two LP filters), two choices of resolution, captures enough periods
  - Cons: none

Note: Also important in deciding upon the 10 kHz and 100 kHz sampling rates was the ability to distinguish 60 Hz noise in the resultant Discrete Fourier Transform (DFT) calculated on the sampled signal. Both 10 kHz and 100 kHz sampling rates give us enough DFT frequency resolution (1.22 Hz & 12.2 Hz, respectively) to distinguish 60 Hz noise and its harmonics.
E. Design Specifications

Packaging

The ADC card will be designed in conformity with the specifications of Dr. Kolbas’ interface box and the previously-manufactured cards. It will be constructed on a 4.5” x 6.5” through-hole board, with an edge connector on one end and a front panel with BNC analog input connection and status LED on the other. The edge connector provides connections to the IEEE-488 signals and +15V/-15V/+5V/+12V power lines on the bus. The IC’s will be mounted in wire-wrap sockets and the connections made via 30 AWG wire-wrap wire. The final product will be similar in appearance to the follow image:

Figure 3: Product Appearance

The following state diagram describes the basic operation of the ADC function card:

![Figure 4: ADC State Diagram](image-url)
The block diagram below shows the basic hardware implementation of the ADC card:

![Block Diagram](image)

**Figure 5: Block Diagram**

**Hardware**

Based on our design decision to implement two sampling rates, two Butterworth low-pass filters (TI UAF42) will be used to anti-alias the +10V to –10V analog input signal in preparation for sampling. One of the filtered signals will be selected by the PIC microcontroller (PIC 18F4515) based on data from the computer over the IEEE-488 bus and routed to the analog-to-digital converter chip (TI ADS7805). The PIC will then direct the ADC chip to sample 8192 data points at the specified rate and will clock the data into the RAM (TI bq4011Y) in big-endian format. When sampling is finished, the card will wait for a signal from the computer and push each byte of the sampled data from the RAM onto the bus via the IEEE-488 protocol. The card will then reset to its “ready” state.

**Software**

The PIC microcontroller will be developed in the PIC MPLAB IDE and programmed in PICmicro assembly language. The flash-programmed PIC will coordinate communication among all the hardware components and control the entire process.
Supporting Calculations

Support for 10 Hz signals
@ 10 kHz sampling rate:

\[
samples \_ per \_ period = \left( \frac{signal \_ period}{sampling \_ period} \right) = \left( \frac{0.1}{0.0001} \right) = 1000
\]

\[
periods \_ captured = \left( \frac{total \_ samples}{samples \_ per \_ period} \right) = \left( \frac{8192}{1000} \right) = 8.192
\]

Support for 25 kHz signals
@ 100 kHz sampling rate:

\[
samples \_ per \_ period = \left( \frac{signal \_ period}{sampling \_ period} \right) = \left( \frac{4 \times 10^{-5}}{1 \times 100^{-5}} \right) = 4
\]

\[
periods \_ captured = \left( \frac{total \_ samples}{samples \_ per \_ period} \right) = \left( \frac{8192}{4} \right) = 2048
\]

The selectable sampling rate allows enough periods of the extreme frequencies to be captured for DFT analysis.

Ability to distinguish 60 Hz

DFT equation:

\[
\Delta f = \frac{f_s}{M}
\]

```
\Delta f = \text{frequency spacing, } f_s = \text{sampling rate, } M = \text{# of samples}
```

```
100 kHz sampling rate, 8192 samples: \Delta f = 12.2 Hz
```

```
10 kHz sampling rate, 8192 samples: \Delta f = 1.22 Hz
```

```
Sufficient frequency resolution to distinguish 60 Hz harmonics on the spectrum
```
F. Design Description

NOTE: See Appendix E for complete detailed schematics.

The following schematic shows a lower-level view of the ADC card:

![ADC Schematic](image)

**Figure 6: ADC Schematic**

Filters

UAF42 filters were utilized to anti-alias the analog input signal before sampling. This UAF42 chip (Universal Active Filter) is manufactured by Texas Instruments and is available in a 14-pin DIP. It accepts input signals in the range of +10 V to –10 V, as required by this project. We used a Burr-Brown DOS filter-design program (Filter42) to configure the filters to their Butterworth low-pass configurations using 1% resistors (see Appendix E for detailed filter schematics).

An external BNC connector on the front panel supplies the input signal to the filters. To prevent excessive 60 Hz noise, a 10 MΩ resistor was placed between the input signal and Special Ground #2 (see Appendix F for interface connections). The UAF42 chips also contain auxiliary op-amps, which we configured as simple followers to present very high input impedances to the incoming signal. The UAF42 chips are powered by +15 V and –15 V from the bus, and are connected to Special Ground #2.
Relay

A Midland Ross double-pole-double-throw (DPDT) latching relay is used to select one of the filtered input signals for input to the ADC (ADS7805). The coils are powered by the +12V from the bus and energized separately by pulses from the PIC to 2N2222A BJT’s, which connect the coils to the +12V Ground:
Analog-to-Digital Converter

The analog-to-digital converter chip (ADS7805) is manufactured by Texas Instruments and is available in a 14-pin DIP. It is a complete 16-bit successive-approximation sampler with sample-and-hold capability. The ADS7805 has a maximum sampling rate of 100 kHz and can output the sampled data byte-by-byte in binary 2's Complement.

A hardware-trim circuit with 1% resistors and tantalum capacitors was constructed around the ADC to allow the Gain and Offset to be calibrated via 10-turn 50 kΩ potentiometers:

![Figure 9: ADC Hardware Trim Schematic](image)

The ADC chip is powered from a dedicated +5V source, which is regulated from the +12 V off the bus. It is connected to Special Ground #1.

![Figure 10: Regulator Schematic](image)

The ADC chip is controlled via signals from the PIC: BYTE is toggled to output the Low Byte or High Byte of the sampled data on Pins 15-22, R/C is pulsed low to initiate a conversion and cause the ADC to release the data lines (to high Z), and BUSY (output from the ADC) rises to notify the PIC that the ADC is ready for another conversion. The CS pin is tied to ground to give full conversion control to R/C.
The relay output is routed to the input of the ADC chip, and eight of the data lines are routed to the SRAM inputs.

**Figure 11: ADC Chip Schematic**

**Memory (SRAM)**

The memory used in this project (32K x 8 BQ4011YMA-70) is manufactured by Texas Instruments and is available in a 28-pin DIP. It is static RAM organized as 32,768 words by 8 bits with 70 ns maximum access time.

The SRAM chip is powered off the +5V digital supply and is connected to the +5V digital Ground. Its address pins are driven by the PIC, as are the \( \text{WE} \) (Write Enable), \( \text{OE} \) (Output Enable), and \( \text{CE} \) (Chip Enable) inputs. Its data pins are driven by the ADC data output, and are also connected to the eight inputs of the octal transparent latch.
Octal Transparent Latch

The 20-pin DIP 74LS373 octal transparent latch allows the SRAM to drive the IEEE-488 bus data lines without sourcing an inordinate amount of current. It is powered off the +5V digital supply and connected to the +5V digital Ground. The $\text{LE}$ (Latch Enable) pin is tied to $V_{CC}$ to enable transparency of the latches, and the $\overline{\text{OE}}$ (Output Enable) pin is connected to $\overline{QT}$ (an active-low output from the Talk/Listen Circuit that indicates when the ADC Card is allowed to drive the bus data lines). Its eight inputs are driven by the SRAM DQ lines, and its eight outputs are connected to data lines D0-D7 on the IEEE-488 bus.
**PIC Microcontroller**

The 40-pin DIP PIC18F4515 is a flash-programmable microcontroller with a maximum of 36 available I/O pins, manufactured by Microchip Technology. We utilized 33 I/O pins and one of the internal 16-bit timer modules. The microcontroller is powered off the +5V digital supply and connected to the +5V digital Ground. The PIC DAVC output drives the base of a 2N2222 BJT to release the IEEE-488 DAV line or pull it to ground. The LEDG and LEDR outputs drive the bases of BJT’s to energize the opposite pins of the bi-color (green and red) status LED. The UNTALK output is connected to the Talk/Listen Circuit to release the IEEE-488 bus data lines when the card is finished transferring the sampled data to the computer. An external clock provides a 40 MHz input to the PIC. (See Appendix H for the connections to each pin.)

**Crystal Clock Oscillator**

The Abracon ACH9502 40 MHz crystal clock oscillator is powered off the +5 V digital supply and connected to the +5 V digital Ground. It provides a 40 MHz clock signal to the PIC to drive the instruction clock. (see Layout for pin connections.)
Talk/Listen Circuit

The Talk/Listen Circuit’s primary function is to receive/send status information to/from the IEEE488 bus interface, and to communicate the card status to the PIC microcontroller. The circuitry consists of three 4-bit magnitude comparators (74LS85), one dual D-type positive edge-triggered flip flop latch, with preset and clear (74LS74), one 8-pin dip switch, several 1kΩ and 10kΩ resistors, and four 2N2222 BJT’s (see Appendix E for schematic). All circuitry is powered off the +5V digital supply and connected to the +5V digital Ground.

The T/L Circuit is designed to read the primary address from the DIP switch (S0-S4) and compare these bits against D0-D4 from the IEEE-488 bus lines. A-9 (ATN/DAV pulse) is also compared against Vcc to determine whether the data on the lines is a command. If the primary address matches that on the lines, and the data is signaled to be a command, the comparators examine D5 and D6. According to the IEEE-488 protocol, D6D5 is 01 to assign the card a Listen status (allow the card to read the data lines). If D6D5 is 10, the card is being assigned a Talk status (allowing the card to drive the data lines).

Upon receiving a Listen assignment, the T/L Circuit pulses A-11 (preset-to-listen) low to signal the box that it acknowledges the assignment. It also utilizes the latch to raise QL (signaling the PIC that the Listen status has been assigned).

Upon receiving a Talk assignment, the T/L Circuit pulls C6 low to signal the box that it acknowledges the assignment. It also utilizes the latch to raise QT (signaling the PIC that the Talk status has been assigned) and lower Q̅T (to enable the octal transparent latch).

If A-10 (Unlisten) pulses high, the card loses its Listen status and drops QL. Similarly, if N-12 (bus reset) pulses low, both the Listen and Talk status are cleared (QL,QT drop and Q̅T rises). When the PIC pulses UNTALK high, the card releases its Talk status, drops QT, and raises Q̅T.
G. Construction Details

This ADC function card was constructed using wire-wrapping technique to provide debugging and modification flexibility to our project sponsor. Some soldering was also utilized for power/ground wires and connections to discrete components. The primary tools used were ORCAD Capture and Microsoft Visio 2003. We divided the soldering and wire-wrapping process into four major Layout sections – Control, Data, Connections, and Other (see Appendix D). The ORCAD drawings (see Appendix E) were used to build the prototype and to draw the pin connections in Visio. Each of the four major Layout categories was printed on a transparency to provide visibility while working on the opposite side of the board.

To construct the ADC Card, begin with a SYNTAX 6.5” x 4.5” through-hole circuit board with edge connector, and attach a custom-built front panel (with BNC connector and bi-color LED) to the other end with epoxy and a card guide. Attach a 7805 voltage regulator to the inside of the front panel (for heat-sinking) and construct the regulator circuit (Figure 10). Solder the 3-layer wire-wrap sockets and the discrete components onto the board as indicated in the Layout (Appendix D).
The next step is to solder and wire-wrap the wires indicated in the Connections layer (30 AWG Kynar-insulated red wire). Once that is accomplished, wire-wrap the Other layer (green wire), Data layer (blue wire), and finally Control layer (yellow wire).

If the individual(s) constructing the board so wish, they may assemble the card in a different manner that allows for modular testing (the process we followed): Construct the filter section as indicated in all layers except Control. Apply input signals to the BNC connector and test the filter outputs with an oscilloscope.

Then proceed to build the Talk/Listen and Octal Transparent Latch circuitry as indicated in all layers except Control. Test this circuit in the interface box by assigning Listen and Talk statuses and observing QL and QT with a logic probe or multimeter.

Construct the ADC circuitry as indicated in all layers except Control. Test this circuit by applying an input signal to the BNC connector and triggering the ADC conversion while probing the data outputs with a digital scope.

Place the SRAM socket and finish the Data Layer. Test the ability of the ADC chip to drive the bus lines by assigning the card a Talk status and observing the ADC chip output on the IEEE-488 data lines.

Finally place the empty PIC microcontroller socket on the board, solder the 40 MHz clock, and finish all layers except Control. Then proceed to wire-wrap all the Control lines. After programming the PIC, place it in the socket.

The IEEE-488 primary address of the card is set via switches 1-5 of the DIP switch. To operate with the provided HP-Basic program, it must be set to binary 28, i.e. 11100 (DIP 5-4 are open and 3-1 are closed). The user may also calibrate the ADC circuitry by applying precise input signals to the card and adjusting the Gain and Offset potentiometers until the sampled data is as expected.

**NOTE:** Wire-wrapping instructions can be found in Appendix P.

**PIC Microcontroller Code**

To program the PIC18F4515 microcontroller with the ADC code, these steps must be followed:

1. Connect the PICSTART PLUS Programmer device with firmware version 04.30.01 or later
2. Start Microchip MPLAB IDE v.7.01
3. Load the “Full3” project (included on CD-ROM): Project ‡ Open ‡ Full3.mcp
4. Insert the PIC18F4515 chip into the PICSTART PLUS
5. Enable the PICSTART PLUS:
   a. Programmer ‡ Select Programmer ‡ PICSTART Plus
   b. Programmer ‡ Enable Programmer
6. Program the chip: Programmer ‡ Program
7. Verify that the Output window indicates success and disable the programmer: Programmer ‡ Disable Programmer
8. Remove the PIC18F4515 chip
9. Close MPLAB IDE and disconnect PICSTART PLUS
H. Costs

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Part Name</th>
<th>Source</th>
<th>Quantity</th>
<th>Our Cost (ea)</th>
<th>Production Cost (ea)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS7805</td>
<td>Analog-to-Digital Converter</td>
<td>Texas Instruments</td>
<td>1</td>
<td>0.00</td>
<td>1.76</td>
</tr>
<tr>
<td>UAF42</td>
<td>Universal Active Filter</td>
<td>Texas Instruments</td>
<td>2</td>
<td>0.00</td>
<td>0.30</td>
</tr>
<tr>
<td>PIC18F4515-I/P</td>
<td>PIC Microcontroller</td>
<td>Microchip</td>
<td>1</td>
<td>0.00</td>
<td>5.61</td>
</tr>
<tr>
<td>BQ4011YMA-70</td>
<td>32x8 SRAM</td>
<td>Texas Instruments</td>
<td>1</td>
<td>0.00</td>
<td>7.50</td>
</tr>
<tr>
<td>DM74L373N</td>
<td>Octal Transparent Latch</td>
<td>Dr. Kolbas</td>
<td>1</td>
<td>0.00</td>
<td>0.40</td>
</tr>
<tr>
<td>74LS85</td>
<td>4-bit Comparator</td>
<td>Dr. Kolbas</td>
<td>3</td>
<td>0.00</td>
<td>0.50</td>
</tr>
<tr>
<td>74LS74</td>
<td>D-Type Flip-Flop</td>
<td>Dr. Kolbas</td>
<td>1</td>
<td>0.00</td>
<td>0.29</td>
</tr>
<tr>
<td>76SB08</td>
<td>8-pin DIP Switch</td>
<td>Dr. Kolbas</td>
<td>1</td>
<td>0.00</td>
<td>1.39</td>
</tr>
<tr>
<td>ED4328-ND</td>
<td>28-pin 0.3&quot; wire-wrap socket</td>
<td>Digi-Key</td>
<td>1</td>
<td>3.20</td>
<td>3.20</td>
</tr>
<tr>
<td>ED4314-ND</td>
<td>14-pin 0.3&quot; wire-wrap socket</td>
<td>Digi-Key</td>
<td>4</td>
<td>1.60</td>
<td>1.60</td>
</tr>
<tr>
<td>ED4628-ND</td>
<td>28-pin 0.6&quot; wire-wrap socket</td>
<td>Digi-Key</td>
<td>1</td>
<td>3.20</td>
<td>3.20</td>
</tr>
<tr>
<td>ED4640-ND</td>
<td>40-pin 0.6&quot; wire-wrap socket</td>
<td>Digi-Key</td>
<td>1</td>
<td>4.58</td>
<td>4.58</td>
</tr>
<tr>
<td>ED4316-ND</td>
<td>16-pin 0.3&quot; wire-wrap socket</td>
<td>Digi-Key</td>
<td>5</td>
<td>1.83</td>
<td>1.83</td>
</tr>
<tr>
<td>2N2222 &amp; 2N2222A</td>
<td>BJT’s</td>
<td>Kolbas &amp; Salas</td>
<td>9</td>
<td>0.00</td>
<td>0.04</td>
</tr>
<tr>
<td>-</td>
<td>1% Resistors &amp; Tantalum Caps.</td>
<td>Mouser</td>
<td>93</td>
<td>0.06</td>
<td>0.06</td>
</tr>
<tr>
<td>-</td>
<td>Capacitors</td>
<td>Rudy Salas</td>
<td>4</td>
<td>0.00</td>
<td>0.05</td>
</tr>
<tr>
<td>-</td>
<td>Resistors</td>
<td>Rudy Salas</td>
<td>20</td>
<td>0.00</td>
<td>0.05</td>
</tr>
<tr>
<td>68WR50K-8510M</td>
<td>Potentiometers</td>
<td>Dr. Kolbas</td>
<td>2</td>
<td>0.00</td>
<td>2.86</td>
</tr>
<tr>
<td>MDT327-218100</td>
<td>DPDT Relay</td>
<td>Dr. Kolbas</td>
<td>1</td>
<td>0.00</td>
<td>8.48</td>
</tr>
<tr>
<td>22541</td>
<td>Blue 30 awg wire-wrap</td>
<td>Jameco</td>
<td>1</td>
<td>4.95</td>
<td>4.95</td>
</tr>
<tr>
<td>22605</td>
<td>Green 30 awg wire-wrap</td>
<td>Jameco</td>
<td>1</td>
<td>4.95</td>
<td>4.95</td>
</tr>
<tr>
<td>22630</td>
<td>Red 30 awg wire-wrap</td>
<td>Jameco</td>
<td>1</td>
<td>4.95</td>
<td>4.95</td>
</tr>
<tr>
<td>22699</td>
<td>Yellow 30 awg wire-wrap</td>
<td>Jameco</td>
<td>1</td>
<td>4.95</td>
<td>4.95</td>
</tr>
</tbody>
</table>

**Support Tools**

<table>
<thead>
<tr>
<th>Source</th>
<th>Our Cost</th>
<th>Production Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>PICSTART PLUS Programmer Device</td>
<td>0.00</td>
<td>200.00</td>
</tr>
<tr>
<td>PICSTART PLUS Firmware Upgrade</td>
<td>29.00</td>
<td>0.00</td>
</tr>
<tr>
<td>IEEE-488 Interface Box</td>
<td>0.00</td>
<td>unknown</td>
</tr>
<tr>
<td>HP 9000/300 series PC</td>
<td>0.00</td>
<td>unknown</td>
</tr>
<tr>
<td>Wire-wrap Tool</td>
<td>0.00</td>
<td>30.00</td>
</tr>
</tbody>
</table>

**Total Cost (w/o shipping)** 80.54 316.72
**Shipping** 26.34 26.34
**Total Cost (w/ shipping)** 106.88 343.06

We were able to obtain a significant number of parts from Mr. Salas and Dr. Kolbas, thus eliminating many expenses. We also obtained free samples from the manufacturers.
I. Conclusions

Our ADC Card was completed successfully and met all the project requirements. This in itself was a surprise result. After completing construction, we only needed to reprogram the PIC microcontroller one time. In addition, we had to replace only one wire to fix a shaky connection.

As a follow-up project, the card could be expanded to operate with the Agilent IEEE-488 cable that would allow the signals to be displayed on a modern PC. We attempted to accomplish this ourselves, but ditched it to concentrate on integrating the card with the HP computer as Design Day approached.
IV. User Instructions

Resources required:

HP 9000/300 PC, IEEE-488 interface box connected via GPIB cable to computer, ADC Function Card,
HP-Basic ADC_FOURIER program

1. Verify that all devices are powered off.
2. Insert the ADC Card into the interface box.
3. Apply power to the computer and the box.
4. Load the HP-Basic ADC_FOURIER program.
5. Apply an input signal to the BNC connector on the card.
6. Chose sampling rate (0 for 10 kHz, 1 for 100 kHz).
Appendices

Appendix A: Project Plan
Appendix B: Block Diagram and Schematic
Appendix C: Critical Design Review
Appendix D: Layout
Appendix E: OrCAD Schematics
Appendix F: Internal IEEE-488 Bus Connections
Appendix G: Timing Diagrams
Appendix H: All Device Pin Connections
Appendix I: PIC Program Flow & Flowchart
Appendix J: PIC Code
Appendix K: HP-Basic ADC_FOURIER Code
Appendix L: Datasheets
Appendix M: Card Specifications
Appendix N: HP-Basic IEEE-488 Commands
Appendix O: Full List of Electronic Components
Appendix P: Wire-wrap Instructions
Appendix Q: Design Software Utilized
Appendix R: ADC Card Pictures