Pins on all devices
(Inputs controlled by PIC are bolded and italicized)

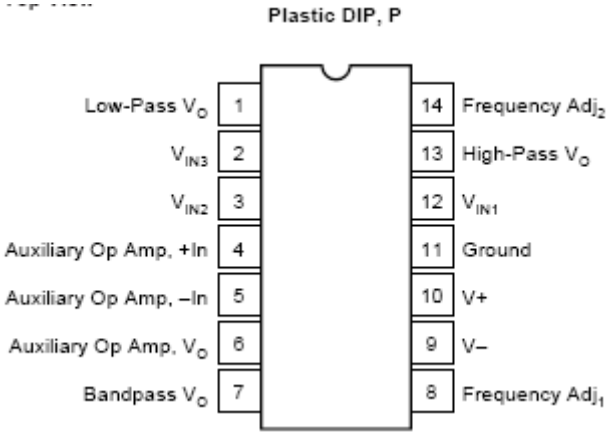
Status LED

***Inputs** (2)*	***PIC RB2, RB3 (Pins 35,36)***

UAF42 Filter

PIN #	Name	Connection
1	Low-pass V_O	ADC V_{IN} (Pin 1)
2	V_{IN3}	from op-amp
3	V_{IN2}	from op-amp
4	Aux. Op Amp, +In	Analog input
5	Aux. Op Amp, –In	Op Amp V_O, ckt
6	Aux. Op Amp, V_O	–In
7	Bandpass V_O	ckt elements
8	Frequency Adj_1	ckt elements
9	V–	–15V
10	V+	+15V
11	Ground	Ground
12	V_{IN1}	ckt elements
13	High-pass V_O	ckt elements
14	Frequency Adj_2	ckt elements

NOTE: This chip requires outside resistors on pins 3, 7, 8, 13, 14, and 12 (circuit will be switched by relay controlled by microcontroller).



ADS7805 ADC chip – **regulate +12V down to +5 V, use a special GND**

PIN #	Name	Connection
1	V_{IN} (analog input)	Filter LP V_O (Pin 1)
2	AGND1	Special GND

3	REF	2.2µF tantalum capacitor to ground
4	CAP	2.2µF tantalum capacitor to ground
5	AGND2	Special GND
6-13	D15-D8 (data byte)	None
14	DGND	Special GND
15	D7/D15	RAM DQ_7 (Pin 19)
16	D6//D14	RAM DQ_6 (Pin 18)
17	D5/D13	RAM DQ_5 (Pin 17)
18	D4/D12	RAM DQ_4 (Pin 16)
19	D3/D11	RAM DQ_3 (Pin 15)
20	D2/D10	RAM DQ_2 (Pin 13)
21	D1/D9	RAM DQ_1 (Pin 12)
22	D0/D8	RAM DQ_0 (Pin 11)
23	***BYTE***	***PIC RA5 (Pin 7)***
24	***R/C_bar***	***PIC RA2 (Pin 4)***
25	CS_bar	Tied low
26	***BUSY_bar***	***PIC RE2 (Pin 10)***
27	V_{ANA}	+5V Analog Supply
28	V_{DIG}	+5V Digital Supply

NOTE: This chip requires an outside circuit (see below).

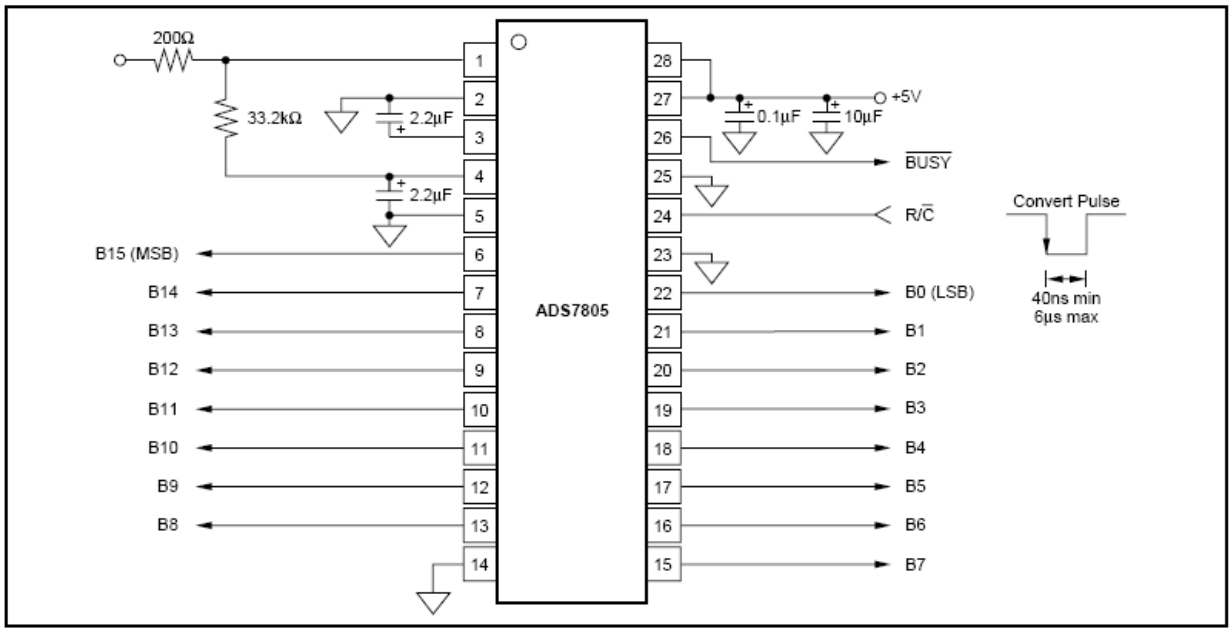


FIGURE 1. Basic Operation.

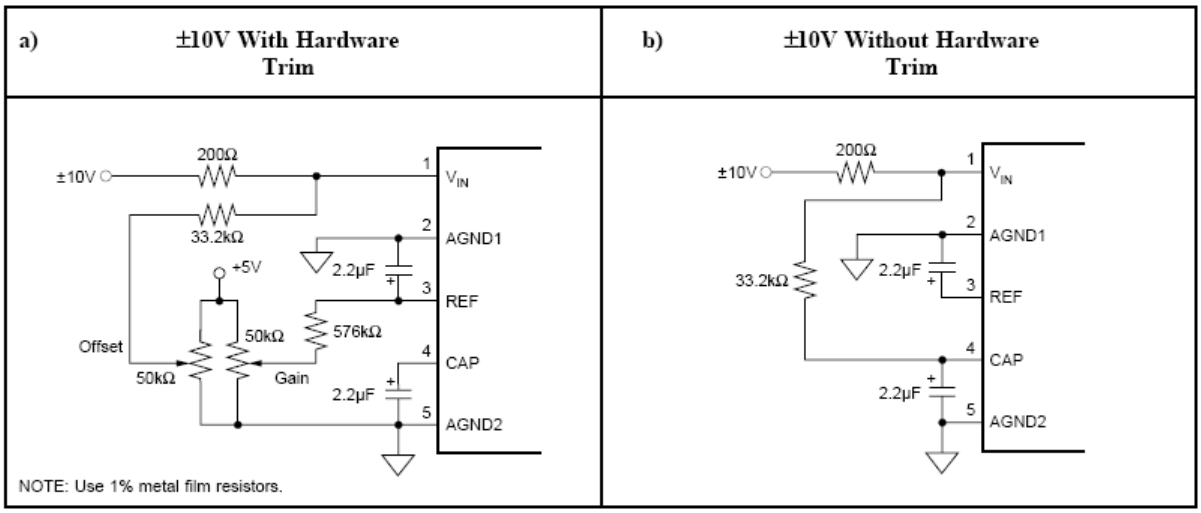
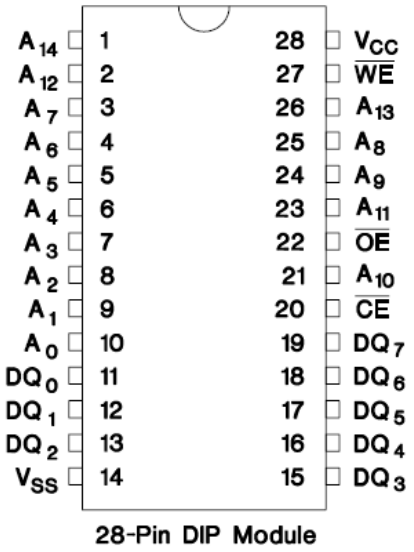


FIGURE 6. Circuit Diagram With and Without External Resistors.

bq4011 SRAM

PIN #	Name	Connection
1	A_{14}	tied to GND
2	***A_{12}***	***PIC RC4 (Pin 23)***
3	***A_7***	***PIC RD7 (Pin 30)***
4	***A_6***	***PIC RD6 (Pin 29)***
5	***A_5***	***PIC RD5 (Pin 28)***
6	***A_4***	***PIC RD4 (Pin 27)***
7	***A_3***	***PIC RD3 (Pin 22)***
8	***A_2***	***PIC RD2 (Pin 21)***
9	***A_1***	***PIC RD1 (Pin 20)***
10	***A_0***	***PIC RD0 (Pin 19)***
11	DQ_0	Latch Pin 3, ADC Pin 22
12	DQ_1	Latch Pin 4, ADC Pin 21
13	DQ_2	Latch Pin 7, ADC Pin 20
14	V_{SS}	Ground
15	DQ_3	Latch Pin 8, ADC Pin 19
16	DQ_4	Latch Pin 13, ADC Pin 18
17	DQ_5	Latch Pin 14, ADC Pin 17
18	DQ_6	Latch Pin 17, ADC Pin 16
19	DQ_7	Latch Pin 18, ADC Pin 15
20	***CE_bar (Chip Enable)***	***PIC RA4 (Pin 6)***
21	***A_{10}***	***PIC RC2 (Pin 17)***
22	***OE_bar (Output Enable)***	***PIC RA3 (Pin 5)***
23	***A_{11}***	***PIC RC3 (Pin 18)***
24	***A_9***	***PIC RC1 (Pin 16)***
25	***A_8***	***PIC RC0 (Pin 15)***
26	***A_{13}***	***PIC RC5 (Pin 24)***

27	***WE_bar (Write Enable)***	***PIC RA6 (Pin 14)***
28	V_{CC}	+5V supply



Talk/Listen Circuit & IEEE-488 lines

PIN	**Description**	**Connection**
QL	***High when listening***	***PIC RA0 (Pin 2)***
QT	***High when talking***	***PIC RE1 (Pin 9)***
QT_bar	Low when talking	Octal OE_bar (Pin 1)
DAV	***Data valid (IEEE488)***	***PIC RE0 (Pin 8)***
NDAC	***Not Data Accepted (488)***	***PIC RC7 (Pin 26)***
NRFD	***Not Ready For Data***	***PIC RC6 (Pin 25)***
D0	***Data Line 0***	***PIC RA1 (Pin 3)***
RESET (C7)	***Go high when IFC received***	***PIC MCLR (Pin 1)***
C4	***Strobes incoming data***	***PIC RB1 (Pin 34)***
UNT	***Untalk***	***PIC RB0 (Pin 33)***

Total PIC I/O Pins used:

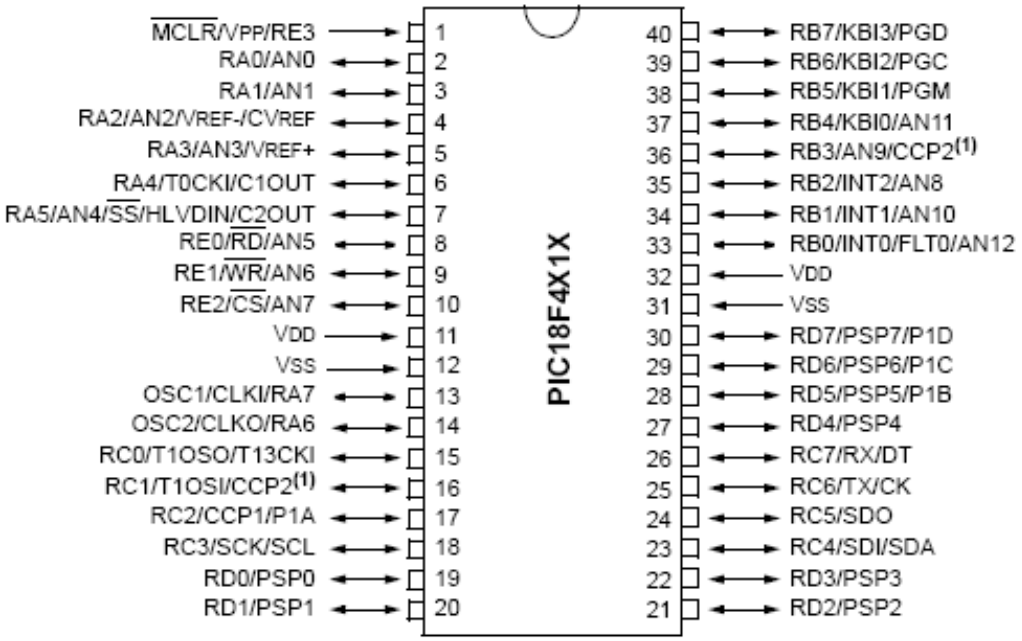
LED:	2	
UAF42:	2 (relay)	
ADS7805:	3	
bq4011:	17	
T/L circuit:	9	
Buffer tri-state:	0	(OE_bar of 74LS373 will be tied to QT_bar)
Total:	33	(35 available)

Appendix H
Project 39 All Device Pins Version 7

PIC18F4515 Microcontroller

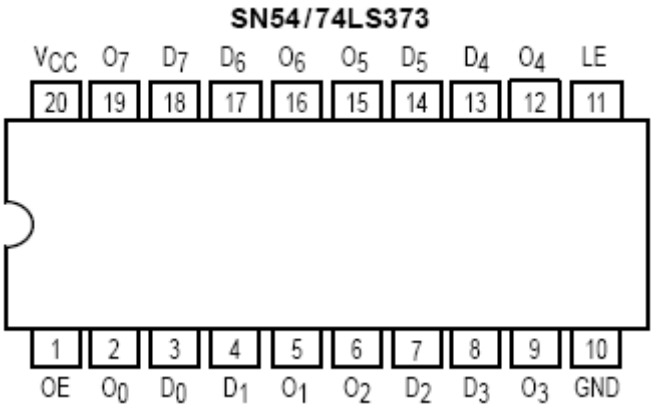
PIN #	Name	Connection
1	MCLR (Master Clear)	RESET (C7 – L12)
2	RA0	QL (L/T, input – 7474 Pin 9)
3	RA1	D0 (L/T, input – 74373 Pin 2)
4	RA2	R/C_bar (ADC, output – Pin 24)
5	RA3	OE_bar (RAM, output – Pin 22)
6	RA4/T0CKI	CE_bar (RAM, output – Pin 20)
7	RA5	BYTE (ADC, output – Pin 23)
8	RE0	DAVC
9	RE1	QT (L/T, input – 7474 Pin 5)
10	RE2	BUSY_bar (ADC, input – Pin 26)
11	V_{DD}	+5 V
12	V_{SS}	Ground
13	RA7/OSC1	40 MHz clock input
14	RA6/OSC2	WE_bar (RAM, output – Pin 27)
15	RC0/T1OSO/T13CKI	RAM A8 (Pin 25)
16	RC1/T1OSI/CCP2	RAM A9 (Pin 24)
17	RC2	RAM A10 (Pin 21)
18	RC3	RAM A11 (Pin 23)
19	RD0	RAM A0 (Pin 10)
20	RD1	RAM A1 (Pin 9)
21	RD2	RAM A2 (Pin 8)
22	RD3	RAM A3 (Pin 7)
23	RC4	RAM A12 (Pin 2)
24	RC5	RAM A13 (Pin 26)
25	RC6	NFRD (R12)
26	RC7	NDAC (R13)
27	RD4	RAM A4 (Pin 6)
28	RD5	RAM A5 (Pin 5)
29	RD6	RAM A6 (Pin 4)
30	RD7	RAM A7 (Pin 3)
31	V_{SS}	Ground
32	V_{DD}	+5 V
33	RB0	UNT (L/T, output – 7474 Pin 3)
34	RB1/INT1	C4 (L9)
35	RB2/INT2	LEDG (output)
36	RB3	LEDR (output)
37	RB4	Relay5k (output)
38	RB5	Relay50k (output)
39	RB6	Unused
40	RB7	Unused

40-pin PDIP



74LS373 octal transparent latch

PIN #	Name	Connection
1	OE_bar	QT_bar from L/T ckt
2	O_0	D0 (R5)
3	D_0	RAM DQ_0 (Pin 11)
4	D_1	RAM DQ_1 (Pin 12)
5	O_1	D1 (R6)
6	O_2	D2 (R7)
7	D_2	RAM DQ_2 (Pin 13)
8	D_3	RAM DQ_3 (Pin 15)
9	O_3	D3 (R8)
10	GND	Ground
11	LE	Tied to V_{CC}
12	O_4	D4 (L5)
13	D_4	RAM DQ_4 (Pin 16)
14	D_5	RAM DQ_5 (Pin 17)
15	O_5	D5 (L6)
16	O_6	D6 (L7)
17	D_6	RAM DQ_6 (Pin 18)
18	D_7	RAM DQ_7 (Pin 19)
19	O_7	D7 (L8)
20	V_{CC}	+5 V


SN54/74LS373
VCC O7 D7 D6 O6 O5 D5 D4 O4 LE
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
OE O0 D0 D1 O1 O2 D2 D3 O3 GND